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Indian Standard

SEMICONDUCTOR DEVICES — INTEGRATED CIRCUITS

PART 2 DIGITAL INTEGRATED CIRCUITS — ESSENTIAL RATING AND CHARACTERISTICS

Section 3 Integrated Circuit Microprocessors

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NEW DELHI 110002

February 1993 **Price Group 3**

Semiconductor Devices and Integrated Circuits Sectional Committee, LT 10

FOREWORD

This Indian Standard (Part 2/Section 3) was adopted by the Bureau of Indian Standard, after the draft finalized by the Semiconductor Devices and Integrated Circuits Sectional Committee had been approved by the Electronics and Telecommunication Division Council.

This standard is one of a series of Indian Standards on integrated circuits and Section 3 of the series of standards on essential ratings and characteristics of digital integrated circuits, covering integrated circuit microprocessors. This is to be read in conjunction with IS 12970 (Part 1) and IS 12970 (Part 2/Sec 1).

This standard (Part 2/Sec 3) is based on IEC Pub 748-2 'Semiconductor devices integrated circuits — Part 2 : Digital integrated circuits' issued by the International Electrotechnical Commission (IEC).

Indian Standard

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS

PART 2 DIGITAL INTEGRATED CIRCUITS — ESSENTIAL RATING AND CHARACTERISTICS

Section 3 Integrated Circuit Microprocessors

1 SCOPE

1.1 This standard applies to microprocessors consisting of a single intergrated circuit. It may also apply to an assembly of integrated circuits designed to function as a microprocessor, but it does not necessarily apply to the individual integrated circuits in such an assembly.

2 REFERENCES

2.1 The Indian Standards listed below are necessary adjunct to this standard:

IS No.	*Title*
1885 (Part 7/Sec 5) : 1971	Electrotechnical vocabulary : Part 7 Semiconductor devices, Sec 5 Integrated circuits and microelectronics
3715 (Part 1) : 1971	Letter symbols for semiconductor devices: Part 1 General aspects (*first revision*)
12970 (Part 1) : 1990	Semiconductor devices—Integrated circuits: Part 1 General
12970 (Part 2/Sec 1) 1992	Semiconductor devices—Integrated circuits: Part 2 Digital integrated circuits — Essential ratings and characteristics, Section 1 General

3 TERMINOLOGY

3.1 For the purpose of the standard, the terms and definitions given in IS 1885 (Part 7/Sec 5) : 1971 and in 3 of IS 12970 (Part 1) shall apply.

4 LETTER SYMBOLS

4.1 For the purpose of this standard, the letter symbols given in IS 3715 (Part 1) : 1971 shall be applicable.

5 CIRCUIT IDENTIFICATION AND DESCRIPTION

5.1 The provisions of **5** of IS 12970 (Part 2/Sec 1) : 1992 shall apply, together with **5.2** of this standard.

5.2 Electrical Compatibility

It should be stated whether the integrated circuit is electrically compatible with other particular integrated circuits or families of integrated circuits, or whether special interfaces are required. Details of the type of output circuit shall be given, for example, three-state, open-collector, etc.

6 FUNCTIONAL SPECIFICATIONS

6.1 Block Diagram

The provisions **6.1** of Sec 1 of this part, apply together with the following:

The block diagram should be sufficiently detailed, to enable the individual functional units within the microprocessor that are affected by the execution of the instructions, to be identified, including the functional blocks that are user-programmable (for example, programmable logic arrays, read-only memory, etc). The main data paths between the functional units and the identification of their external connections should be also shown.

6.1.1 *Identification of Terminals*

The following terminals should be identified on the block diagram:

- supply terminals, that is, terminals intended to be connected to the power supplies;
- intput or output terminals, that is, terminals into which or out of which signals pass. The term 'signal' includes pulse and more complex waveforms;
- input/output terminals, that is, terminals that may function at different times as input or output terminals;

- Three-state output terminals, that is, output terminals that may be controlled to give a high-impedance condition.

6.2 Functional Description

The following information should be given:

a) size, in bits, of word; that is, processed;

b) memory addressing range for each type of memory for which a separate addressing procedure is used, for example, external or internal memory, read/write or read only memory;

size, in bits, of word addressed in each type of memory, where this is different from that in item '(a)' above;

c) size, in bits, of the address;

d) number, types and size in bits and words of internal registers, both programme addressable and otherwise, for example, general purpose accumulator, index, programme counter, stack pointer, stack register, control register, arithmetic/logic unit, condition code register;

NOTE — The condition codes give information about the result of arithmatic or logic operation, such as zero, result, parity, sign, carry, overflow, etc.

e) modes of memory addressing provided, for example, immediate, direct, relative, indexed;

f) types of interrupt capability provided, for example, programme enabled/disabled, vectored and otherwise;

g) methods of transferring input and output data and output of addresses, for example, whether serial, parallel or a combination of both;

h) whether the microprocessor microprogrammable or not;

j) method of generating clock signals; and

k) operation mode, static or dynamic.

6.3 Instruction Set

A comprehensive list should be given of the instructions that may be performed by the microprocessor. This should give the instruction code, instruction mnemonic, the operation(s) that result from the execution of the instructions including any condition codes or register contents that are affected, the number of clock cycles and preferably also the number of machine cycles required and, where appropriate, the number of propramme words used to form the instruction and addressing mode capabilities for each instruction.

6.3.1 This information may be given for each instruction or for each group of similiar instructions. Differences should be indicated when these occur due to alternative modes of addressing.

6.4 Configuration of Instructions

Where appropiate, the format of the intsructions used should be distinguished to indicate the bit organisation of the intsruction words. This should be given in the form of a diagram as follows:

- operation code field;
- address mode field;
- register definition field; and
- operand field.

6.5 Input and Output Signals

The function of each input and output signal should be stated. In general, the signals may be divided into:

- data signals;
- address signals; and
- control signals;

As a minimum, control signals exist that define when the data transfer is to be performed, the direction, the direction of transfer (that is, into or out of the microprocessor), and should include a reset input signal that forces the microprocessor into a defined state.

Examples of additional control signals that may be provided are:

a) *Bus Control Signals*

- to specify when the address bits are stable and present valid information;
- to specify whether the address is to memory or a peripheral device;
- to control the function of the bus when there is time multiplexing of signals; and
- a ready signal controlled by the addressed memory.

b) *Executive Control Signals*

- holds request;
- hold acknowledge; and
- priority handling.

c) *Other Control Signals*

- interrupt in (maskable);
- interrupt in (not maskable);
- interrupt acknowledge;
- wait state output;
- output disable; and
- synchronization, etc.

7 RATINGS (LIMITING VALUES)

7.0 The ratings given must cover the operation of the microprocessor over the specified range of operating temperatures. Where such ratings are temperature-dependent, this dependence should be indicated.

7.1 Electrical Limiting Values

7.1.1 *Power Supply Voltage(s)*

a) Maximum value(s) and polarity(ies).

b) Maximum value of the voltage between a common supply terminal and case or reference terminal, where appropriate;

c) Sequence of application and/or removal of supply voltages, where appropriate. Any restriction on the duration of the sequence should be stated.

7.1.2 *Input Voltages*

Maximum values, with respect to a common reference terminal (and polarities, where appropriate)

7.1.3 *Input Currents* (*Where Appropriate*)

Maximum values.

7.1.4 *Output Voltages*

Maximum values, with respect to a common reference terminal (and polarities, where appropriate).

7.1.5 *Output Currents*

Maximum values.

7.2 Temperatures

a) Minimum and maximum ambient or reference-point operating temperatures.

b) Minimum and maximum storage temperatures

c) Maximum value and duration of lead temperature.

7.3 Power Dissipation

Maximum values.

8 RECOMMENDED OPERATING CONDITION (WITHIN THE SPECIFIED OPERATING TEMPERATURE RANGE)

8.1 Power Supply Voltage(s)

Polarity, nominal value and tolerance(s) for each power supply voltage.

8.2 Clock Inputs

a) Minimum and maximum values of low and high level voltages;

b) Minimum and maximum values of rise and fall times;

c) Minimum and, where appropriate, maximum values of clock period;

d) Minimum and, where appropriate, maximum values of pulse duration. For multi-phase clock input, this information should be given for each input;

e) For multi-phase clock inputs, minimum and, where appropriate, maximum values of delays between successive phases of clock phases.

8.3 Input Voltages (Excluding Clock Inputs)

Minimum and maximum values of low and high level voltages.

8.4 Output Currents

Maximum and, where appropriate, minimum values for both low and high level output voltage conditions.

8.5 External Elements (Where Appropriate)

Value(s) and tolerance(s) of any external elements recommended or specified for use with the microprocessor.

8.6 Set-up and Hold Times

Minimum and/or maximum values, as appropriate, for each input (or group of inputs) relative to the appropriate transition of a clock pulse, for specified values of:

- clock pulse rise and fall time;
- input voltage at other terminals.

Value should be stated to enable the critical timing requirements for each independent function of the microprocessor to be established by the user.

8.7 Timing Diagrams for Control Sequences

Minimum duration of input signals, and their timings relative to the clock signal(s) for input sequences necessary to bring the microprocessor into a predetermined state, for example, restart (or reset), interrupt, hold, etc. These should be related to the sequences for execution of programme instructions.

These sequences should be expressed in terms of clock cycles and preferably also in terms of machine cycles.

9 ELECTRICAL CHARACTERISTICS

9.1 Static Characteristics

Each electrical characteristic of **9.1.1**, **9.1.2**, **9.1.3**, and **9.1.4** below should be stated under specified electrical worst-case condition with respect to the recommended range of supply voltage(s), as stated in **8.1** and:

a) over the specified range of operating temperatures, or

b) at a temperature of 25°C, and at a maximum and minimum operating temperatures.

9.1.1 *Power Supply Current(s)*

a) Static operation

Typical and maximum values of current drawn from each power supply for normal operation and, where appropriate, standby operation, for specified values of:

— supply voltage(s); and
— clock frequency.

This information should also be given for clock inputs acting as pulsed power supplies.

b) Dynamic operation.

Typical values should also be given for the above information either at a different clock frequency or as curve (or curves) versus clock frequency.

9.1.2 *Input Currents (Including Clock Inputs)*

Maximum value(s), where appropriate, under both low and high level input voltage conditions, for specified values of:

— supply voltage(s);
— input voltage; and
— input voltage(s) at other terminals.

This information should also be given for those inputs that may also function as outputs.

9.1.3 *Output Voltages*

Maximum value of low level and minimum value of high level output voltage for specified values of:

— supply voltage(s);
— load current; and
— input voltage(s) (where appropriate).

This information should also be given for those outputs that may also function as inputs.

9.1.4 *Output Off-State Currents*

For three-state outputs that may be disabled so as to give neither a low-level nor a high-level output condition: maximum value in the off-state condition for specified values of:

— supply voltage(s);
— continuous voltage at the relevant terminal; and
— input voltages at other terminals.

9.1.5 *Capacitances*

Maximum values of capacitances at clock input, input and output terminals, for specified values of:

— supply voltage(s);
— continuous voltage at the relevant terminal;
— frequency; and
— input voltages at other terminals.

9.2 Dynamic Characteristics

Each electrical characteristic of **9.2.1** should be stated under specified electrical worst-case conditions with respect to the recommended range of supply voltage(s) as stated in **8.1**.

Limit values as required in **9.2.1** or, if these are not mutually acceptable to manufacturer and user, typical values should be stated either:

a) over the specified range of operating temperatures, or

b) at a temperature of 25°C, and at maximum and minimum operating temperatures.

Alternatively 'b' should be used only if the worst-case value of the characteristic over the whole temperature range can be deduced from the values given at the specified temperatures.

In all cases, limit values applicable at 25°C should be stated.

9.2.1 *Times Characterizing the Response of the Circuit*

9.2.1.1 *Propagation times*

The following times should be stated under specified conditions (*see* Note 1):

a) t_{PHL} — propagation time with output going to low level, maximum value;

b) t_{PLH} — propagation time with output going to high level; maximum value.

If there are several different logic information paths, separate times should be specified for each path.

Additional times should be given, where appropriate, for three-state outputs entering and leaving the high-impedance state.

9.2.1.2 *Transition times*

Transition times should be stated under specified conditions (*see* Note 1) as follows:

a) If the typical value of transition time is comparable to (*see* Note 2), or greater than, the typical value of propagation time, a maximum value of transition time should be stated.

b) If the typical value of transition time is less than 10 ns a minimum value should be stated (*see* Note 3);

c) If both conditions (a) and (b) are fulfilled, then both minimum and maximum values should be stated.

Transition times, when required, should be stated for both directions off transition (that is, t_{THL} and t_{TLH}).

NOTES

1 The specified conditions of measurement should include the characteristics of the input pulse and oscilloscope (or other appropriate measuring system) and the configuration and component values of the output loading network.

2 The transition time is considered comparable to propagation time if its value exceeds 50 percent of the value of propagation time.

3 The object here is to state when very short transition times may be obtained which may give rise to overshoot and coupling problems using practical loads.

10 MECHANICAL RATINGS, CHARACTERISTICS AND OTHER DATA

10.1 Any specific mechanical or environmental rating applicable to the particular microprocessor should be stated.

See also **5.5** of IS 12970 (Part 1)

11 SUPPLEMENTARY INFORMATION

11.1 Output Loading Capability

The maximum number of specified loads that can be driven from each output. This information may be given for more than one type of load.

11.2 Noise Margins

Information about the microprocessor that enables noise margins to be calculated is given in **8.2** and **9.1.3** of this section (*see also* **17.2** of Section 1 of this part).

11.3 Applicable Data

Additional information concerning the variations of the characteristics in **9** with supply voltage, load impedance, etc, may be given.

Further information, detailing the action of each instruction, may be given to supplement that in **6.3**. In particular, this should give details of sequences and operations involved in programme branching and interrupts.

Further information detailing the function and sequences of operations of each input or group of input may be given to supplement that in **6.3** and **8.7**. This may include state diagrams and timing diagrams.

Information on instruction execution times may be given for particular instructions such as binary addition or register-to-register transfer. If an average time is given, details of the instruction used and the memory access time should be included.

11.4 Other Information

A statement should be given whether the integrated circuit contains internal protection against high electrostatic voltages or electrical fields.

12 HANDLING PRECAUTIONS

See **8** of IS 12970 (Part 1).

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